Short Papers

Yield Sensitivity of HEMT Circuits to Process Parameter Variations

Jogendra C. Sarker and John E. Purviance

Abstract—**This work summarizes the use of a graphical tool, yield factor histograms, to study the yield sensitivity of HEMT circuits to process parameter variations. A computer program called SPICENTER is used to incorporate the HEMT statistical physical model with a SPICE circuit model and then to generate the yield factor histograms and yield sensitivities as functions of the process parameters. This work presents, for the first time, the application of these tools to microwave circuits. Two example HEMT circuits, a 2-input NOR gate and an inverter chain, illustrate the concepts. Yield sensitivity is presented as yield percent change per parameter percent change.**

Nomenclature

- L Gate length.
- Z Gate width.
- q Electronic charge.
- μ Low field mobility of two-dimensional electron gas.
- β Charge control coefficient.
- δ Effective width of conduction channel.
- ϵ Permittivity of AlGaAs.
- E_c Saturation electric field of two-dimensional electron gas.
- v_s Saturation velocity of two-dimensional electron gas.
- g_m Transconductance parameter.
- C_{gs} Gate to source capacitance.
- f_T Current gain cut-off frequency.
- Q_T Total charge.
- λ Channel length modulation parameter.
- V_{DS} Externally applied drain to source voltage.
- V_{GS} Externally applied gate to source voltage.
- V_{tho} Threshold voltage for two-dimensional electron gas.
- V_D Drain to source voltage.
- V_G Gate to source voltage.
- I_D Drain to source current.
- R_S Parasitic source resistance.
- R_D Parasitic drain resistance.

I. Introduction

The study of circuit performances and their sensitivities to process parameter variations is necessary to avoid failure of costly and time-consuming circuit designs. Most engineers study the sensitivity of their circuits with the linear variation of the process parameters, one parameter at a time. Due to the statistical fluctuations in the mechanical, thermal, chemical and optical processes used in fabrication, these variations are actually random and all the variations occur simultaneously. For this reason single parameter, linear sensitivity studies may be inadequate [1].

In the past, not much work has been done to study the sensitivity of the HEMT circuit performances with the statistical variation of the process parameters. In our previous work [2], based on dc and CAD small-signal models [3], [4] and using the Monte Carlo technique, we have studied the statistical sensitivity of four different isolated HEMT devices to process parameter variations. In this work, we have chosen those models for the HEMT device to study the statistical sensitivity of two basic HEMT circuits.

Section II-A shows the basic structure of a HEMT device and the model parameters used in the dc model. Section II-B gives the equations used for the small-signal parameters derived in reference [4]. In Section III, we briefly discuss the circuit performance yield and the yield sensitivity. This material comes from many references, see [1], [5] for example, and was further developed in [2]. It is concisely presented here for completeness and convenience. Section IV discusses the Monte Carlo process parameter simulator. In Section V, the example circuits are discussed and the results are presented. In this short paper we are only addressing yield sensitivity and its efficient calculation, not yield optimization or sensitivity reduction, which are applications and extensions of this work.

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The authors are with the NASA Space Engineering Research Center, Department of Electrical Engineering, University of Idaho, Moscow, ID 83843.

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II. HEMT Model

A. DC Model

A complete description of the dc model is given in [4]. It is briefly developed here. The basic structure of a uniformly doped AlGaAs/GaAs HEMT is shown in Fig. 1. Based on this structure and using Trofimenkoff type velocity-field linear relation [6], Wang and Ku [3] modeled the I-V characteristics for both normal and compressed transconductance regions. In their model for the normal linear region, there are three model parameters which are directly related to the physical parameters and these parameters are given below.

$$A = \frac{Zq\beta\mu}{L} \tag{1}$$

$$B = LE_c \tag{2}$$

$$C = \frac{L^2}{2\epsilon Z v_s \delta}. \tag{3}$$

B. Small-Signal Model

From Wang's dc model, we have analytically derived the expressions for g_m, C_{gs} and f_T in the normal linear region [4]. For the linear region:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{AV_D}{1 + \frac{V_D}{B}} \tag{4}$$

$$C_{gs} = \frac{\partial Q_T}{\partial V_G} = \frac{AL^2\left(2 + \frac{V_D}{B}\right)}{\mu} \tag{5}$$

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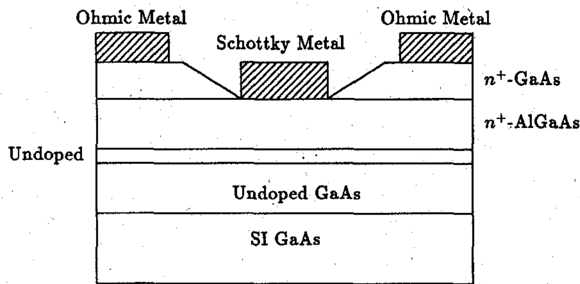

Fig. 1. Schematic diagram of a uniformly doped AlGaAs/GaAs HEMT.

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{\mu V_D}{2\pi L^2\left(1 + \frac{V_D}{B}\right)\left(2 + \frac{V_D}{B}\right)}. \tag{6}$$

For the saturation region, we apply numerical techniques to solve the associated derivatives. See [4] for details.

Another parameter "BETA", which is used in the JFET SPICE circuit model, is calculated from the relation

$$\text{BETA} = \frac{g_m}{2(1 + \lambda V_{DS})(V_{GS} - V_{tho})}. \tag{7}$$

Based on these analytical and numerical expressions we have calculated these parameter values for a given bias condition as a function of the process parameters L, Z and μ.

III. Statistical Analysis

A. Yield and Yield Sensitivity

Circuit performance yield and yield sensitivity as a function of process parameter variations are the important criteria which we wish to study. A recent development of yield and yield sensitivity is given in [2].

We will assume that the circuit performance of interest is completely described by a set of parameters, $(x1, x2, \cdots xn)$, denoted X. Yield, Y, can be expressed as the expectation value of $A(X)$:

$$\begin{aligned} Y &= E\{A(X)\} \\ &= \int_{-\infty}^{+\infty} A(X)p(X)\, dX \\ &= \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}\cdots\int_{-\infty}^{+\infty} A(x1, x2, \cdots, xn) \\ &\quad \cdot p(x1, x2, \cdots, xn)\, dx1\, dx2 \cdots dxn \end{aligned} \tag{8}$$

where $0 \leq E\{A(X)\} \leq 1$ and

$$A(X) = \begin{cases} 1 & \text{if circuit gives acceptable performance with parameter } X \\ 0 & \text{if circuit does not give acceptable performance with parameter } X \end{cases}$$

and $p(X)$ is the parameter joint probability density function.

Monte Carlo techniques are usually used to estimate the value of the yield integral. It would be useful to take the derivative of Y with respect to the density parameters (not explicitly shown in these expressions) to develop a yield sensitivity. But general derivative expressions are complicated and numerically expensive. However, an approximation is presented in the next section which allows the estimation of the yield derivative for all parameters of interest, using only one M-point Monte Carlo simulation. The presentation is essentially the same as given in [2].

B. Yield Factor and its Derivative

Here, we wish to numerically evaluate the yield as a function of each of the process parameter values, $(x1, x2, \cdots, xn)$. This can be approximated by developing a yield factor which is given by

$$\begin{aligned} Y(xio) = \int_{x1}\cdots\int_{xi-1}\int_{xi+1} &\cdots\int_{xn} A(x, x2, \cdots, xi-1, xio, xi+1, \cdots, xn) \\ &\times p(x1, x2, \cdots, xi-1, xio, xi+1, \cdots, xn) \\ &dx1 \cdots dxi-1\, dxi+1 \cdots dxn \end{aligned} \tag{9}$$

where $Y(xio)$ is the yield with all parameter values varied statistically according to $p(X)$, except for the ith parameter which is fixed at the value, xio. This is equivalent to letting the probability density function

$$\begin{aligned} &p(x, x2, \cdots xi-1, xi, xi+1, \cdots xn) \\ &\quad = \delta(xi - xio)p(x1, x2, \cdots, xi-1, xio, xi+1, \cdots, xn) \end{aligned} \tag{10}$$

where $\delta(xi - xio)$ is the Dirac delta function. This approximation to $p(X)$ has significant numerical benefits, as will be shown. However, calculating yield (or yield sensitivity) using this approximation can induce error. If the variation of xi is small, or if the yield is not a strong function of xio, then this error is small. Otherwise care must be taken in interpreting the yield factors.

Now, if $Y(xio)$ is essentially constant as xio varies through its allowed range of values, its tolerance range, then the yield factor, and hence the yield is not sensitive to the ith parameter. Therefore, the sensitivity of the yield with respect to the parameter values is estimated by determining the slope of the yield factor. Analytically, the yield factor sensitivity is given as

$$\begin{aligned} \frac{\partial Y(xio)}{\partial xio} = \frac{\partial}{\partial xio}\Bigg[\int_{x1}\cdots\int_{xi-1}\int_{xi+1} &\cdots\int_{xn} A(x1, x2, \cdots, xi-1, xio, xi+1, \cdots, xn) \\ &\times p(x1, \cdots, xi-1, xio, xi+1, \cdots, xn) \\ &dx1 \cdots dxi-1\, dxi+1 \cdots dxn\Bigg] \end{aligned} \tag{11}$$

The authors have found yield factor sensitivity to be an accurate and reliable estimate of yield sensitivity.

To better calculate the yield factor and its derivative, an unbiased estimator of $Y(xio)$, $\hat{Y}(xio)$ is used. The $\hat{Y}(xio)$ is defined as

$$\hat{Y}(xio) = \frac{1}{M}\sum_{j=1}^{M} A(Xj) \tag{12}$$

where xi is a sample of the process parameters, sampled according to $p(X)\ \delta(xi - xio)$, i.e., the ith component of X is fixed at xio and all other parameters are allowed to vary according to $p(X)$.

The implementation is simplified by dividing the acceptable values of xi into nine equal regions, called "BINS". An estimate of $Y(xio)$, for all xio, is developed by performing one Monte Carlo analysis where all process parameters of interest are allowed to vary according to $p(X)$. Nine yield factors are simultaneously cal-

culated for all the parameters by keeping track of which BIN the value of *xio* lies, for all *i* in the Monte Carlo trials. A printout of the Monte Carlo estimation of $\hat{Y}(xio)$ versus the *xio* BIN's is called a yield factor histogram. Detailed discussion on the implementation technique is given in reference [5]. The estimated yield sensitivity is calculated by determining the slope of the yield factor histograms.

IV. Monte Carlo Simulator and the HEMT Circuit Sensitivity

A. Process Parameters of Interest

In this work, we have chosen the TRW #2078 HEMT [3] to implement the two example circuits. This TRW #2078 HEMT shows only the normal transconductance effect. Only five parameters, A, B, C, D and V_{tho} are needed in the model. D is a parameter used to model the threshold voltage shift of the two dimensional electron gas caused by the drain voltage. The model parameters are explicitly functions of the process parameters such as gate length, L, gate width, Z, carrier mobility, μ etc. So, in a yield sensitivity study one should statistically vary all the parameters which are directly or indirectly related to the manufacturing process and identify the parameters to which the yield is most sensitive. We have simultaneously varied three process parameters, gate length, gate width and the mobility of the carriers to compute the performance yield. The mobility of the carriers is temperature dependent [7] and also it varies as the gate bias fluctuates [8]. To include the temperature and bias voltage fluctuations we have chosen this parameter as one of the parameters of interest.

The model parameters $q\beta$, E_c and $1/2\epsilon v_s\delta$ are kept constant in this work. The values of these parameters are derived by using the nominal values given in Table I [2]. Then putting the values of these constants back in the model parameter equations (1)–(3) we can write the model parameters as functions of L, Z and μ. These model parameter expressions are then used directly in the Monte Carlo simulator.

The dc model does not include the parasitic R_D and R_S effects. We have chosen statistical variation of R_D, R_S and the threshold voltage V_{tho} in the circuit model. So, in our Monte Carlo analysis, six parameters, L, Z, mobility, R_D, R_S and V_{tho} are simultaneously varied.

B. Monte Carlo Simulator and the SPICENTER Program

In our Monte Carlo analysis we have randomly varied L, Z, μ, R_D, R_S and V_{tho} simultaneously. We have chosen a $\pm 5\%$ uniform, independent variation of the parameters about their nominal values listed in Table I. This statistical model has not been verified at this time and the results of a study like this can be affected by the type of statistical parameter model used. It is likely that L and Z are correlated, which is not accounted for in this work.

The random parameter values are used in the model program to calculate the small-signal parameters, g_m, C_{gs} and BETA for a specific bias condition. To create 1000 statistical HEMT's, 1000 simulations are performed. These 1000 HEMT parameter values form a Truth Model [9] input to the JFET SPICE circuit model. In the SPICE model, R_D, R_S and V_{tho} are the independent parameters while C_{gs} and BETA are the dependent parameters calculated from L, Z and μ. The gate-to-drain capacitance C_{gd} is very small compared to C_{gs} ($\approx$ 30 fF). We estimated C_{gd} as 5 fF and keep it constant in the analysis.

For the Monte Carlo analysis, SPICENTER takes each set of parameter values created from the model program and computes the circuit performance. The circuit performances calculated from the simulation are compared with the nominal performance specification. If the circuit meets the specification then the circuit is accepted otherwise it is rejected. From the accounting of the accepted circuits, the program creates the yield factor histograms for each of the independent parameters L, Z, μ, R_D, R_S and V_{tho}. The procedure we used in our study is shown in Fig. 2.

The sensitivity of the performance yield was determined by linear fitting of the yield factor histograms and then calculating the slope of the linear fit. The values of the slopes are presented as yield%/parameter %.

TABLE I.
Physical Parameter Nominal Values of the TRW #2078 HEMT

Parameter	Value
$L(\mu m)$	0.35
$Z(\mu m)$	65
$V_{tho}(V)$	−0.017
$A(mA/V^2)$	49.517
$B(V)$	5.285
$C(K\Omega)$	8.341
D	0.015
$R_S(\Omega)$	5.9
$R_D(\Omega)$	6.0
$\mu(m^2/Vs)$	0.44

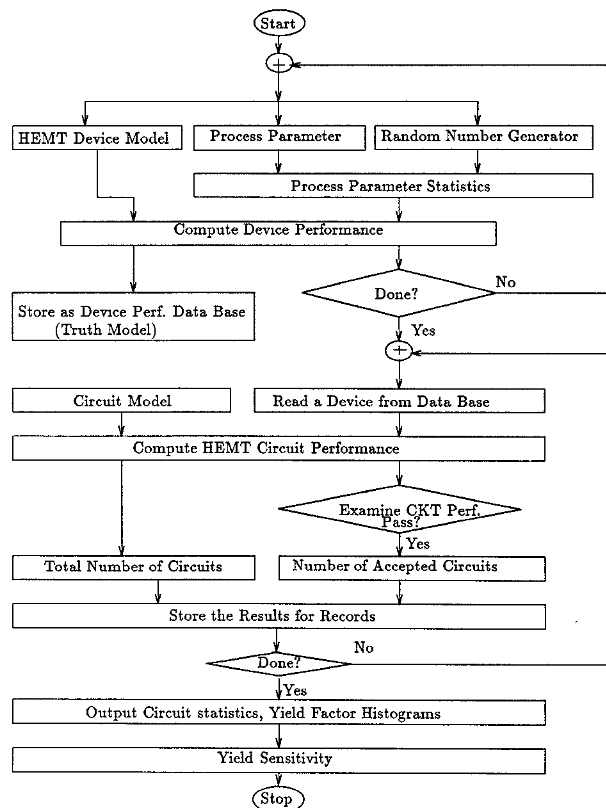

Fig. 2. Algorithm of the Monte Carlo process parameter simulator.

V. Results

In this work, we have chosen two example HEMT circuits to illustrate the use of the yield factor histograms to study the yield sensitivity to process parameter variations.

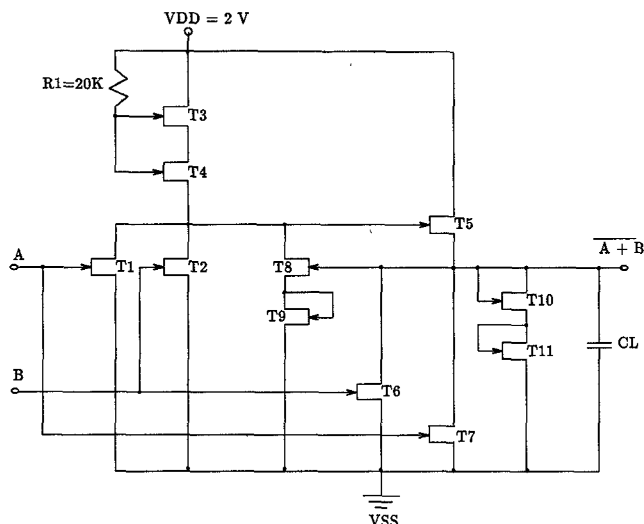

Fig. 3. Circuit diagram of an FFL HEMT NOR gate.

A. Example I: 2-Input NOR Gate with Feedback FET Logic

Our first example circuit is a 2-input NOR gate with feedback FET Logic (FFL), shown in Fig. 3 [10]. It is two to four times faster than the comparable GaAs direct-coupled FET logic. The primary feature of FFL is the push-pull output stage which works in conjunction with the feedback transistor T8. Without feedback, the output transistor T5 would remain fully on after the output high state is reached. The feedback transistor turns off the output transistor after the output reaches high, thus it saves dc power. Another function of the feedback transistor is to clamp the output voltage at a level that is just high enough to turn on the next gate, but no so high as to waste power or to add additional gate delay. All of the transistors in the circuit are n-channel type transistors.

The performance criterion chosen for this NOR gate circuit was the delay time. The delay time determines the speed of the circuit, so it is one of the important criteria of a digitial circuit. In our analysis, the delay time was defined as the time taken at the output to attain 90% of its final steady state value from the instant the input is triggered with a step voltage. The "nominal" value of this delay time was calculated by using the nominal values of the parameters.

Fig. 4 shows the yield factor histograms generated by SPICENTER for 1000 simulations of the circuit. As we can see from the figure the yield is very sensitive to the device gate length and it goes down as the gate length increases. The gate width and the carrier mobility variations give higher yield for larger width and for higher mobility. From our study, we found that the yield is almost independent of the parasitic resistances, R_D and R_S and the device threshold voltage. The sensitivities of the yield with respect to each parameter were calculated by linear fitting of the yield factor histogram and these are given in Table II.

B. Example II: HEMT Inverter Chain with Complementary Logic

In both microwave and digital circuits, the inverter is the basic gain stage of all microwave amplifiers. We propose a chain of five HEMT inverters implemented with complementary logic [11]. Fig. 5 shows the circuit diagram. P1 through P5 are the p-channel and N1–N5 are the n-channel type HEMTs. We arbitrarily choose the output capacitance values of 0.1 pF. A step voltage of magnitude 1 V is applied as input Vin and we observe the output across the

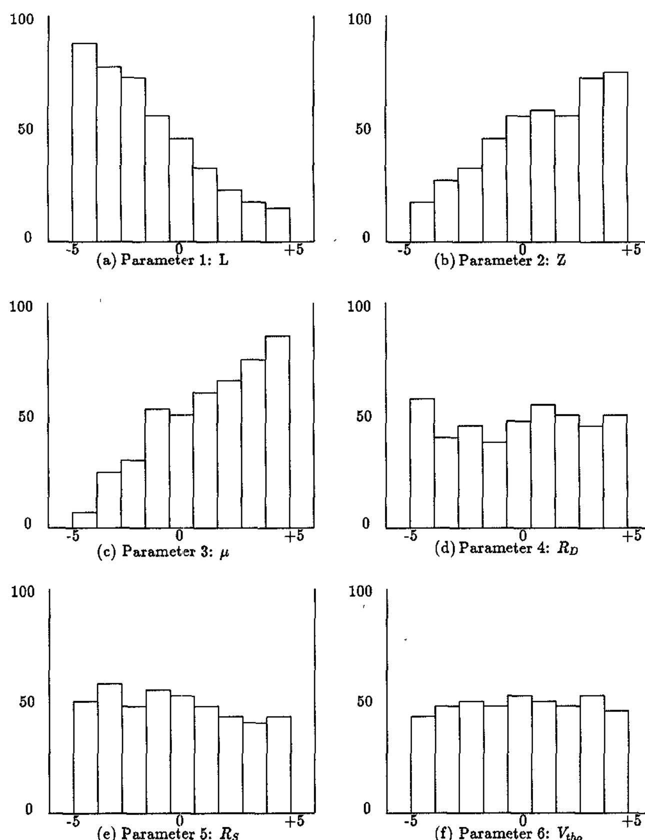

Fig. 4. Yield factor histograms, yield% versus parameter% of FFL NOR gate.

TABLE II
YIELD SENSITIVITY OF 2-INPUT NOR GATE WITH FEEDBACK FET LOGIC

Parameter	Yield Sensitivity (yield%/parameter%)
Parameter 1 : L	-9.03 ± 0.51
Parameter 2 : Z	$+6.36 \pm 0.47$
Parameter 3 : μ	$+8.06 \pm 0.62$
Parameter 4 : R_D	$+0.15 \pm 0.78$
Parameter 5 : R_S	-1.58 ± 0.48
Parameter 6 : V_{tho}	$+0.24 \pm 0.42$

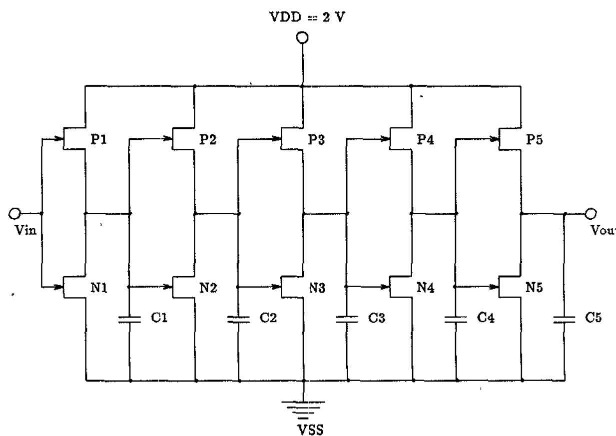

Fig. 5. Circuit diagram of a complementary HEMT inverter chain.

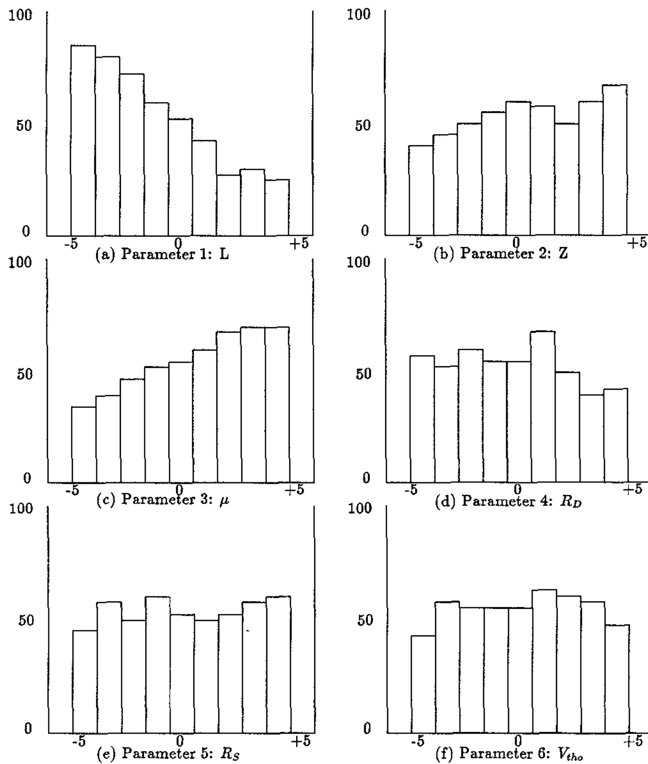

Fig. 6. Yield factor histograms, yield% versus parameter% of complementary HEMT inverter chain.

TABLE III
YIELD SENSITIVITY OF HEMT INVERTER CHAIN WITH COMPLEMENTARY LOGIC

Parameter	Yield Sensitivity (yield%/parameter%)
Parameter 1 : L	-7.56 ± 0.49
Parameter 2 : Z	$+2.25 \pm 0.54$
Parameter 3 : μ	$+4.12 \pm 0.29$
Parameter 4 : R_D	-1.62 ± 0.87
Parameter 5 : R_S	$+0.86 \pm 0.62$
Parameter 6 : V_{tho}	$+0.62 \pm 0.71$

capacitor C5. Here also we have used the TRW #2078 HEMT's for both p- and n-channel HEMT's.

For the inverter chain, we have chosen the risetime of the output at C5 as the performance specification. The risetime is defined as the time taken by the output signal to rise from 10% to 90% of its final steady state in response to a step voltage applied at the input. For this circuit, the risetime is specified to be less than 16.85 psec.

1000 simulations were performed for the inverter chain. In Fig. 6, we present the yield factor histograms of this circuit. The yield sensitivities were calculated and are given in Table III. For this circuit, we observed similar results as the NOR gate. But in this case, the yield sensitivity with respect to L, Z and mobility is less as compared to example I. Again the yield is almost insensitive to R_D, R_S and V_{tho} of the device.

VI. CONCLUSION

This work uses the yield factor histograms to study the yield and the yield sensitivity of HEMT circuits with process parameter variations. From our statistical Monte Carlo analysis of two example circuits, we observed that the yield is sensitive to the device dimension and to the carrier mobility and almost insensitive to the threshold voltage.

The analysis technique we present in this paper will help the microwave circuit designer to efficiently calculate yield sensitivity to process parameter variations.

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REFERENCES

[1] J. E. Purviance and M. D. Meehan, "A sensitivity figure for yield improvement," *IEEE Trans. Microwave Theory Techniques*, vol. 36, pp. 413–417, Feb. 1988.

[2] J. C. Sarker and J. E. Purviance, "Yield sensitivity study of Al-GaAs/GaAs high electron mobility transistor," *Int. J. Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 2, pp. 12–27, Jan. 1991.

[3] G. W. Wang ang W. H. Ku, "An analytical and computer-aided model of the Al-GaAs/GaAs high electron mobility transistor," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 657–663, May 1986.

[4] J. C. Sarker and J. E. Purviance, "DC and small-signal physical models for the al-GaAs/GaAs high electron Mobility transistor," in *Proc. 3rd NASA Symp. VLSI Design*, Moscow, ID, Oct. 1991.

[5] A. MacFarland, J. E. Purviance, D. Loescher, K. Diegert, and T. Ferguson, "Centering and tolerancing the components of microwave amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1987, pp. 633–636.

[6] F. N. Trofimenkoff, "Field-dependent mobility analysis of the field-effect transistor," in *Proc. IEEE*, vol. 53, pp. 1765–1766, Nov. 1965.

[7] K. Hilosaka, Y. Hirachi, T. Mimura, and M. Abe, "A Microwave power double-heterojunction high electron mobility transistor," *IEEE Electron Device Lett.* vol. EDL-6, pp. 341–343, July 1985.

[8] S. M. Liu, M. B. Das, W. Kopp, and H. Morkoc, "Determination of 2-D electron-gas carrier mobility in short gate-length MODFET's by direct elimination of parasitic resistance effects." *IEEE Electron Device Lett.*, vol. EDL-6, pp. 594–596, Nov. 1985.

[9] M. Meehan and T. Wandinger, "Accurate design centering and yield prediction using the truth model," in *IEEE Microwave Theory Tech. Symp. Dig.*, June 1991, pp. 1201–1204.

[10] D. E. Fulkerson, "Feedback FET logic: a robust, high-speed, low-power GaAs logic family," *IEEE J. Solid-State Circuits*, vol. 26, pp. 70–74, Jan 1991.

[11] M. Shur, *GaAs Devices and Circuits*. New York: Plenum, 1987.

Analytic Physics-Based Expressions for the Empirical Parameters of the Statz-Pucel MESFET Model

S. D'Agostino, G. D'Inzeo, P. Marietti, L. Tudini, and A. Betti-Berutto

Abstract—**In this paper we present a novel approach to the evaluation of the dc parameters of a semi-empirical MESFET model: starting from the analytical expression of the drain current derived from a physics-based model, previously proposed, we provide a method to calculate**

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The authors are with the Department of Electronic Engineering, University "La Sapienza" of Rome, Via Eudossiana 18, 00184 Rome, Italy.

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